

Lógica Combinacional Modular

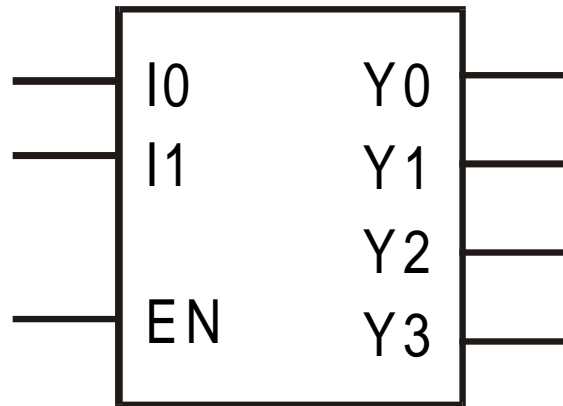
(Parte I)

Prof. Luis Araujo

Sistemas Digitales

<http://www.ing.ula.ve/~araujol/sd>

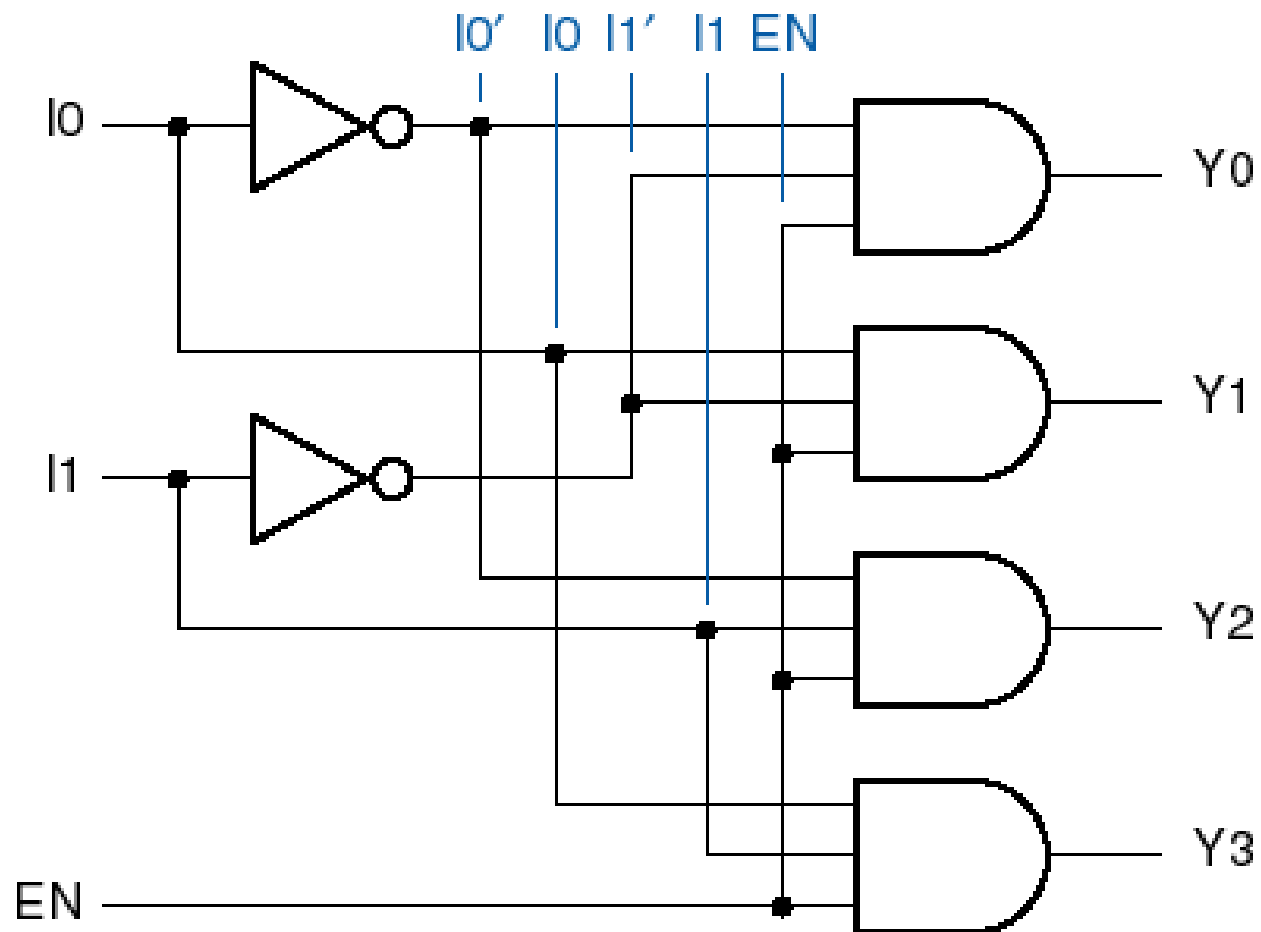
Decodificadores



<i>Inputs</i>			<i>Outputs</i>			
EN	I1	I0	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

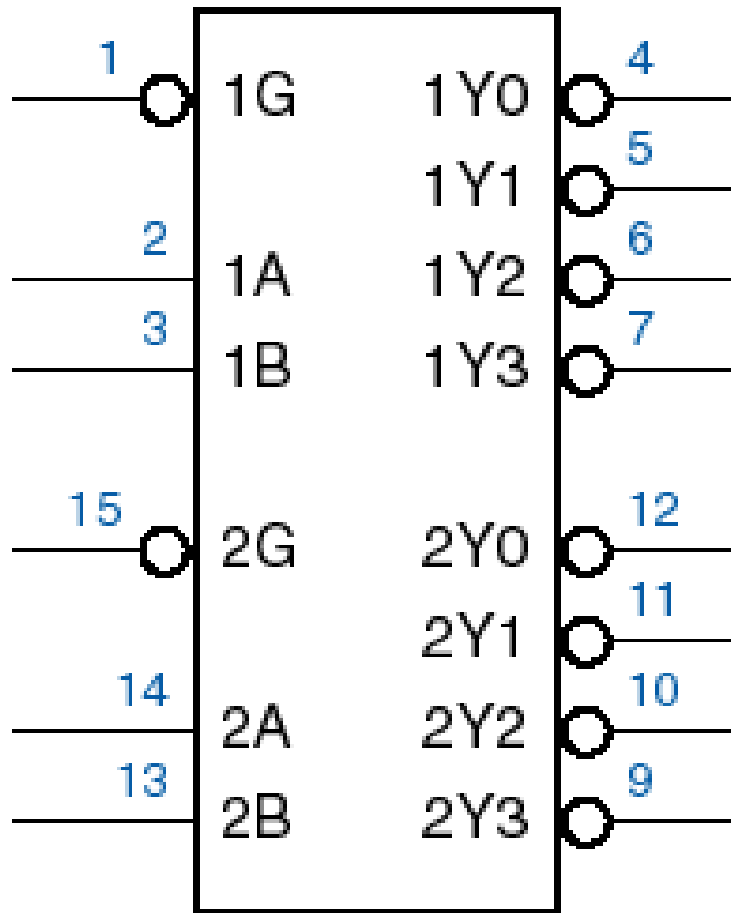
Nota: “x” condición no importa

Diagrama Interno

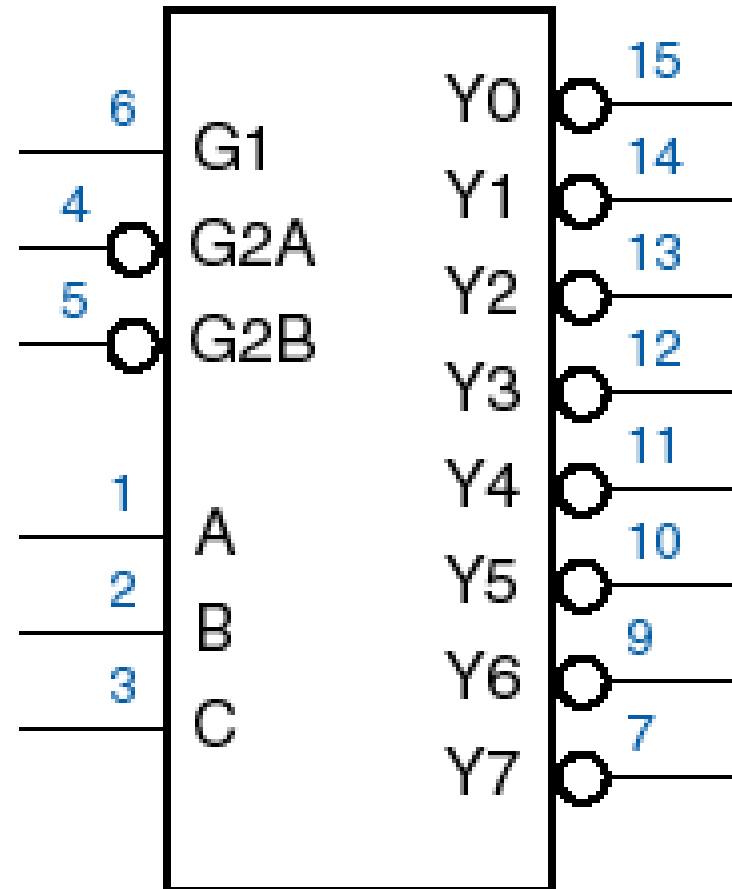


Decodificadores Comerciales

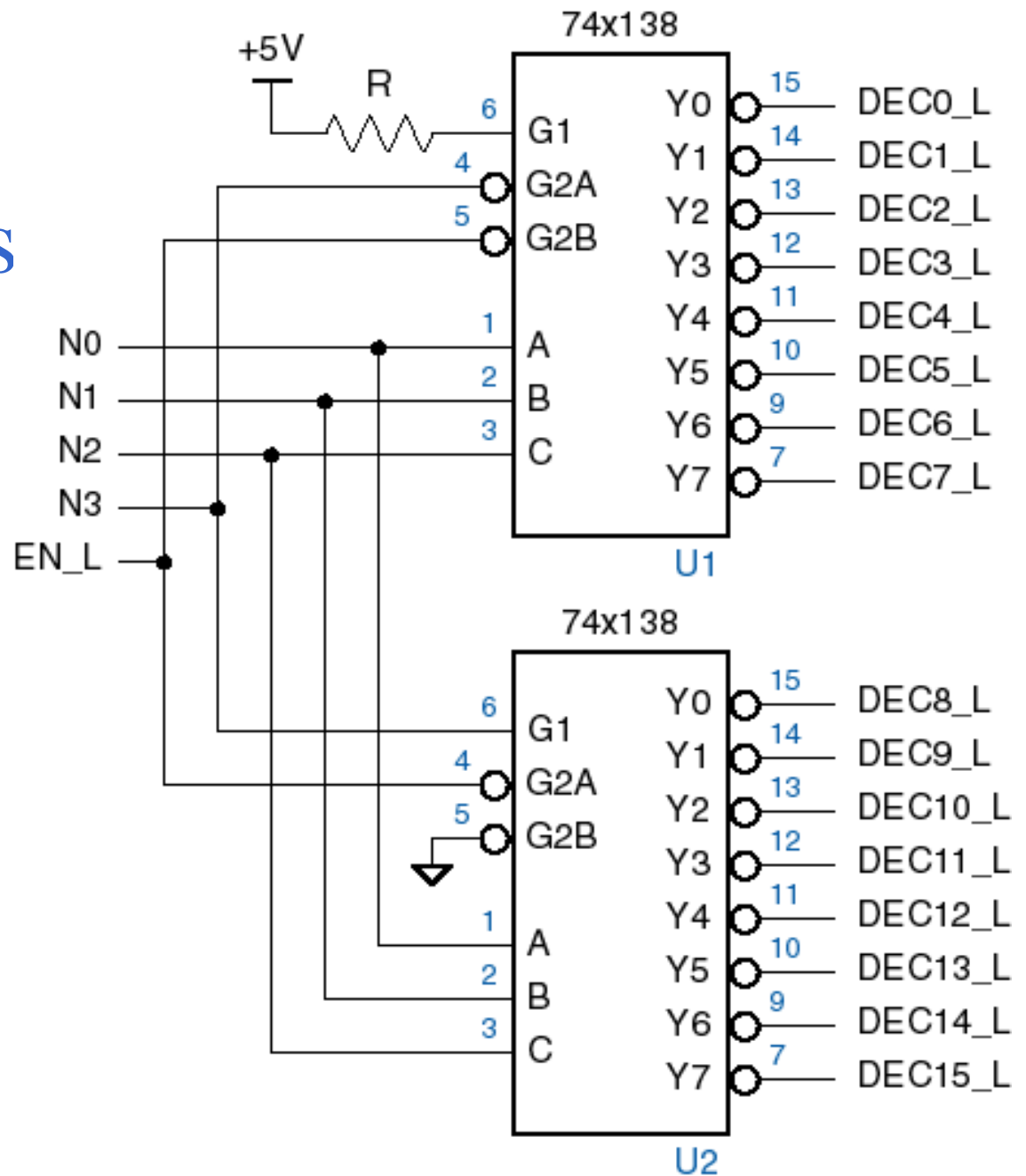
74x139



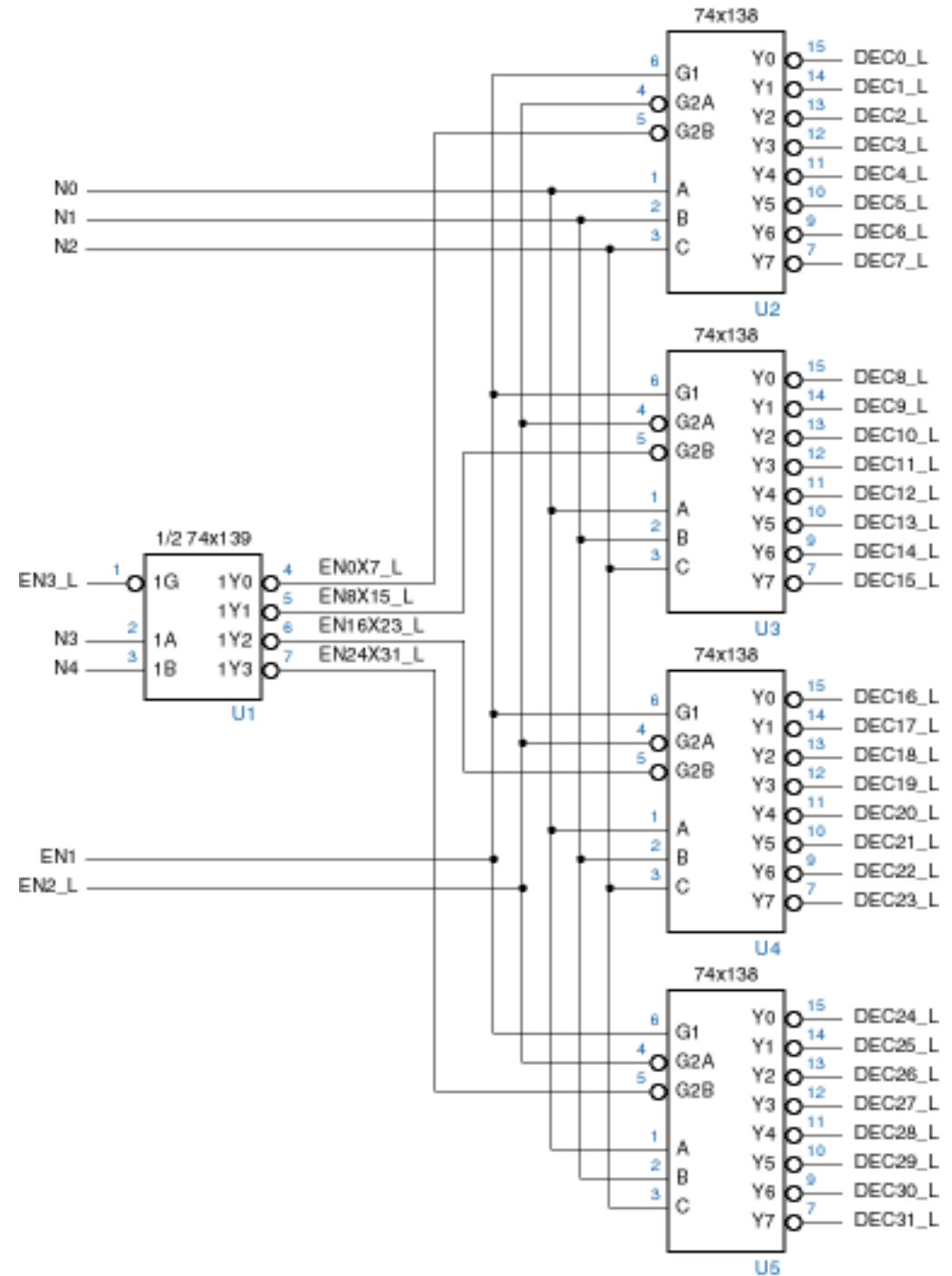
74x138



Expansión de Decodificadores



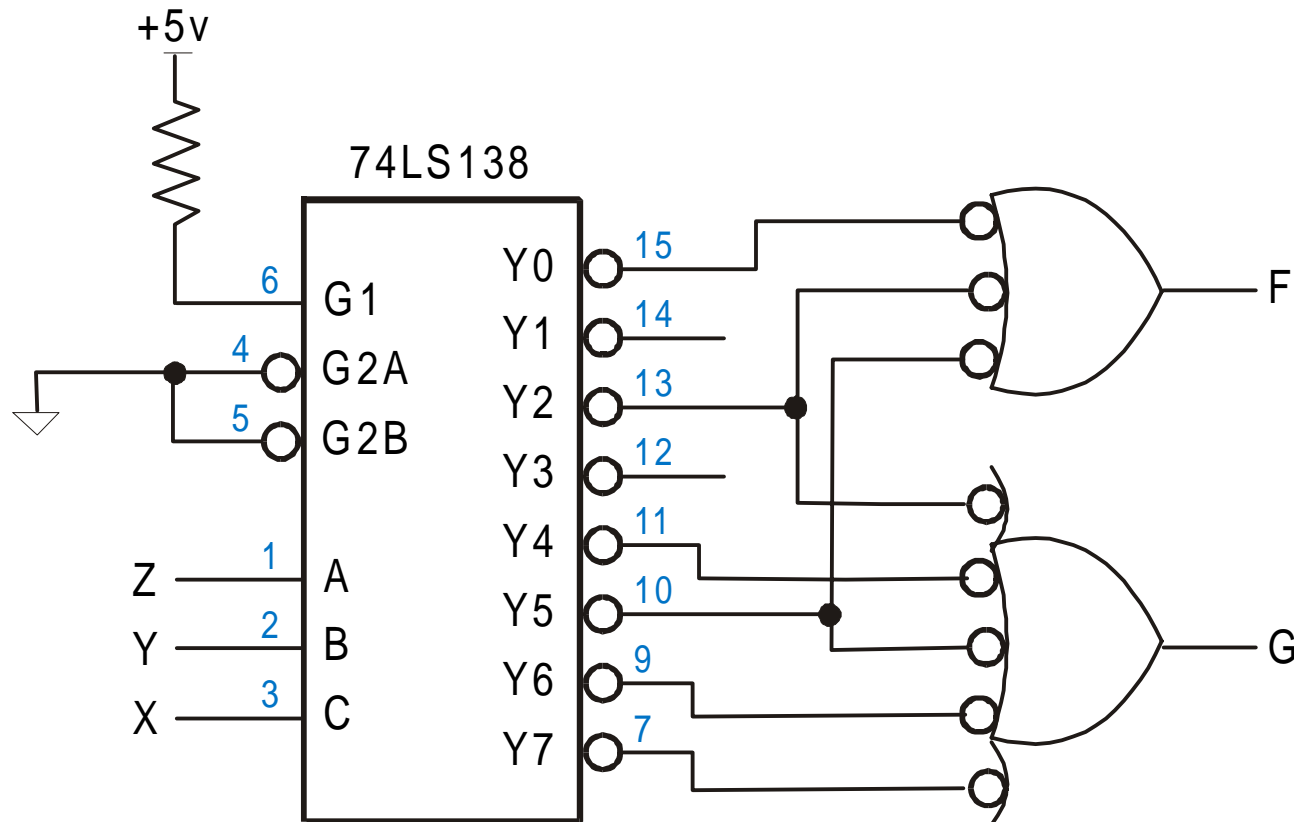
Expansión de Decodificadores



Funciones con Decodificadores

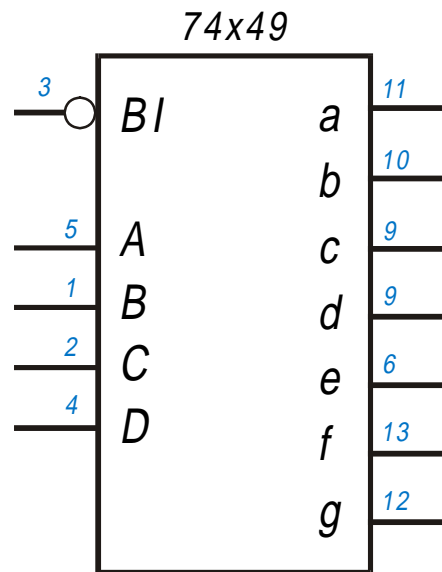
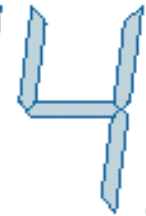
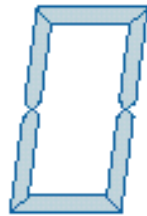
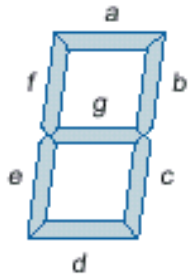
$$f(x, y, z) = \sum m(0, 2, 5)$$

$$g(x, y, z) = \sum m(2, 4, 5, 6, 7)$$

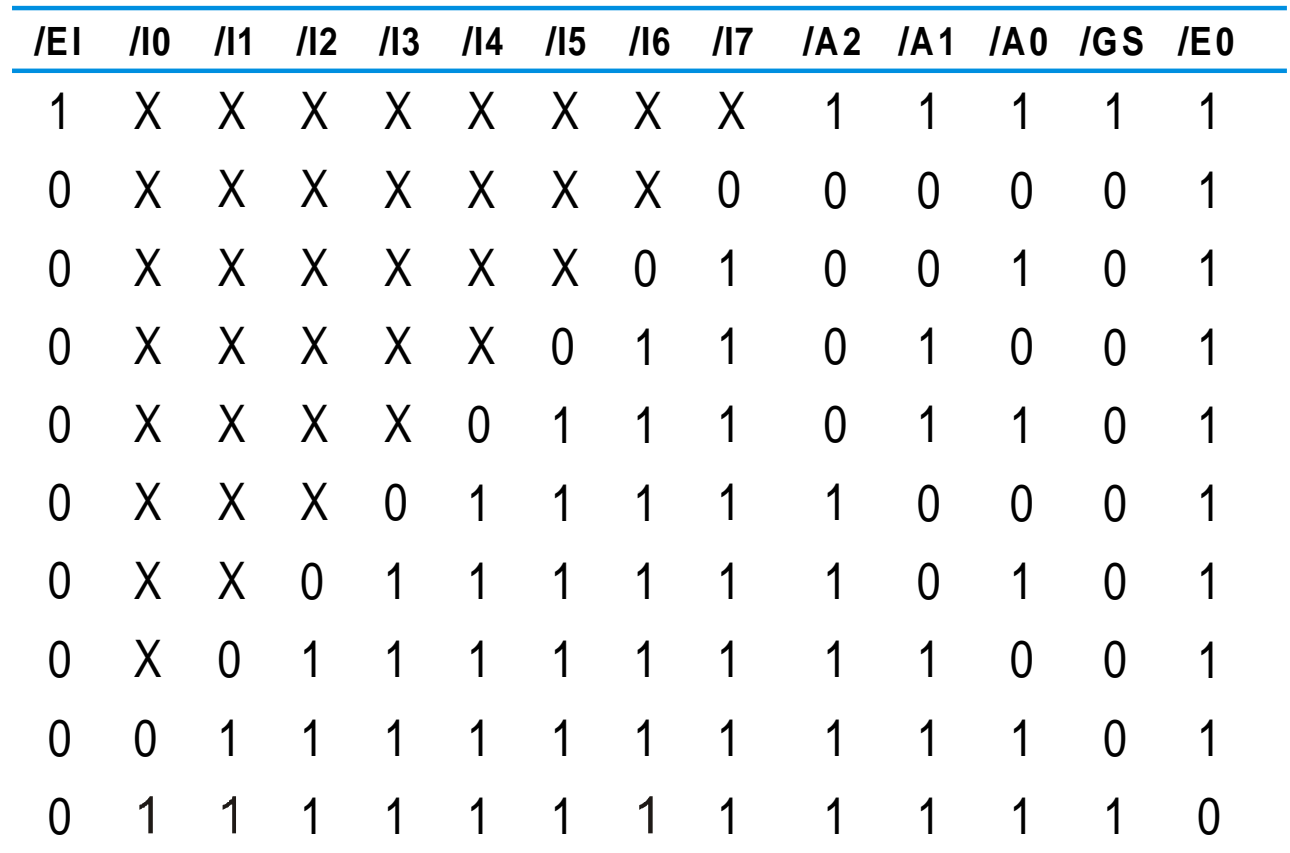


Decodificador 7 segmentos

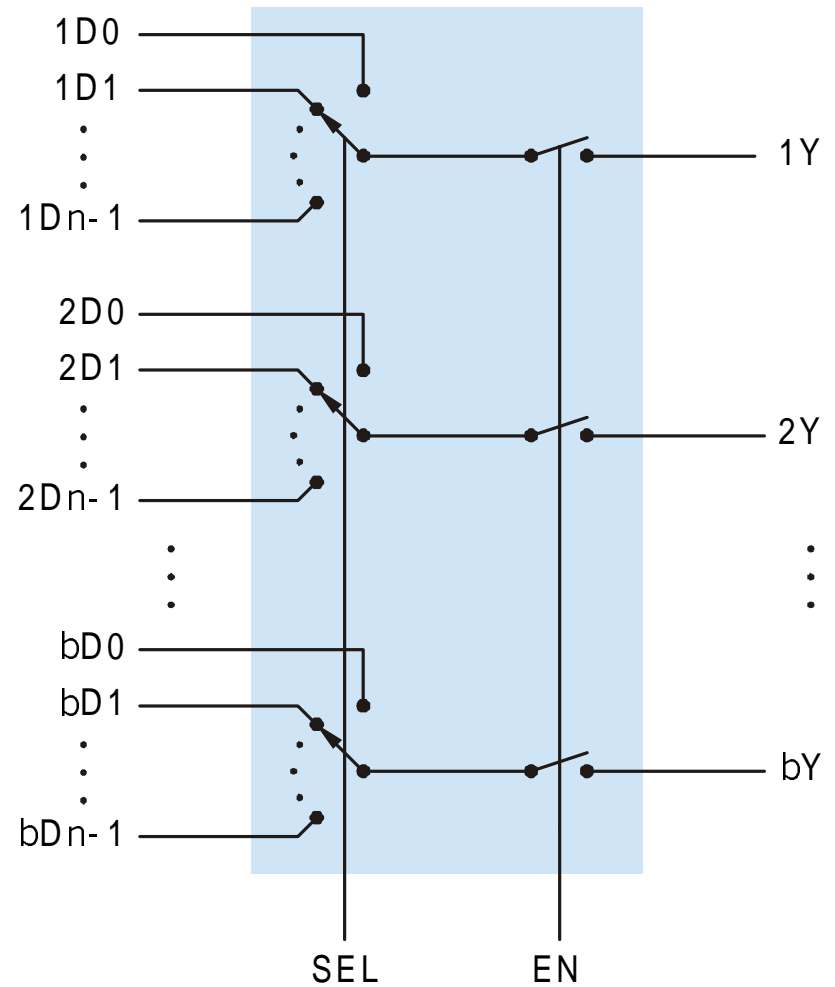
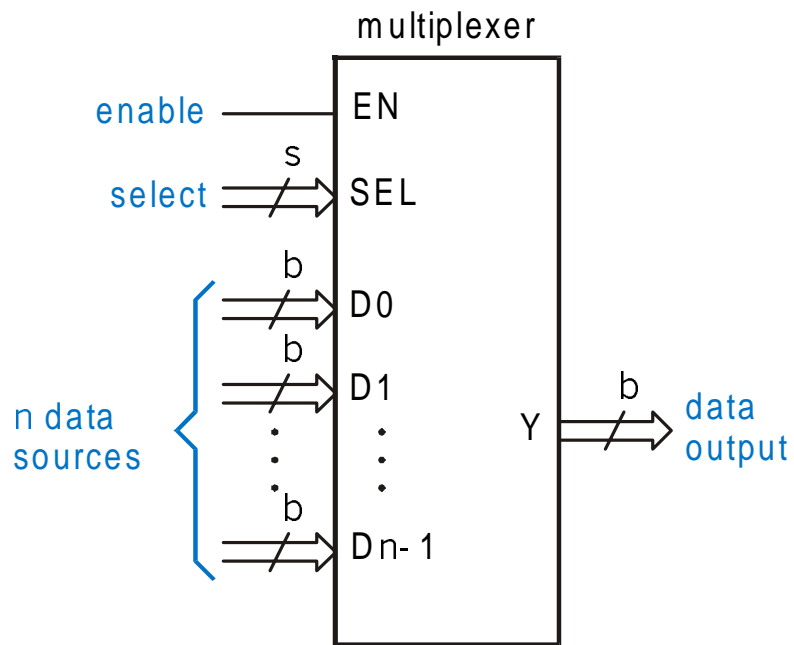
Display 7 Segmentos



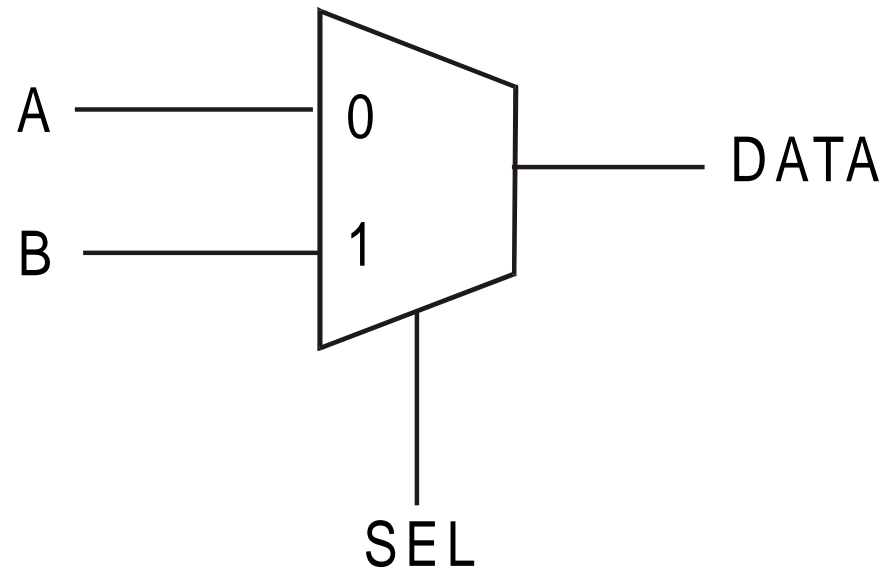
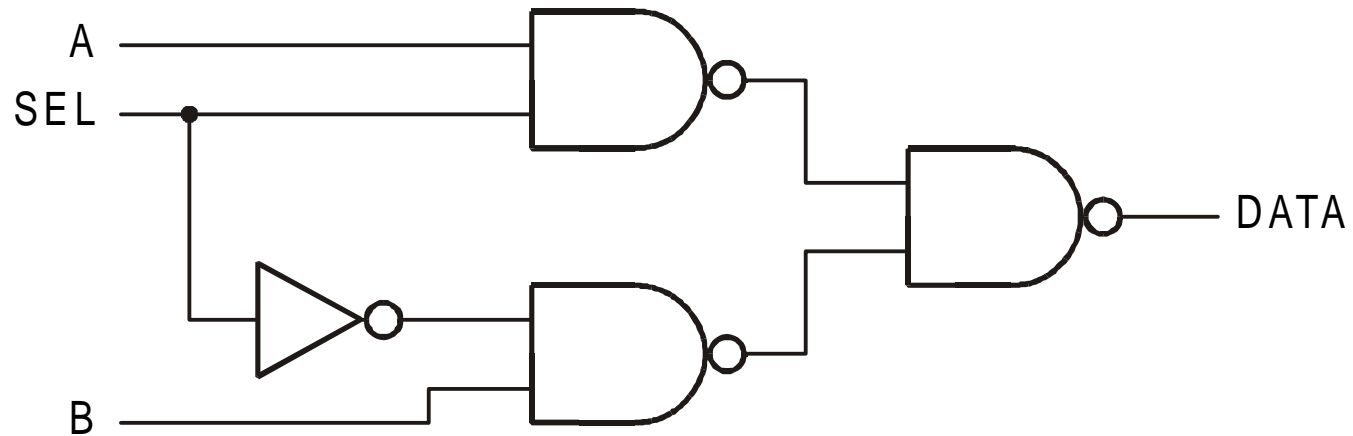
Codificador de Prioridad



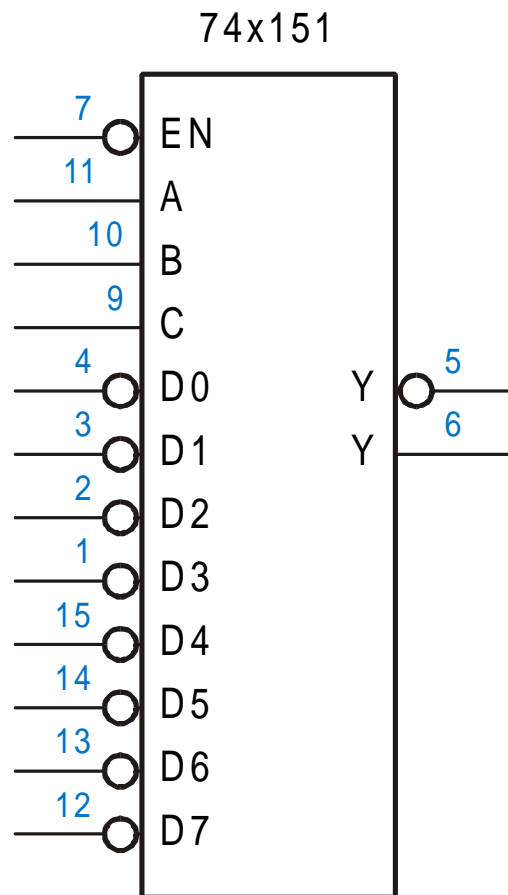
Multiplexores



Estructura Interna

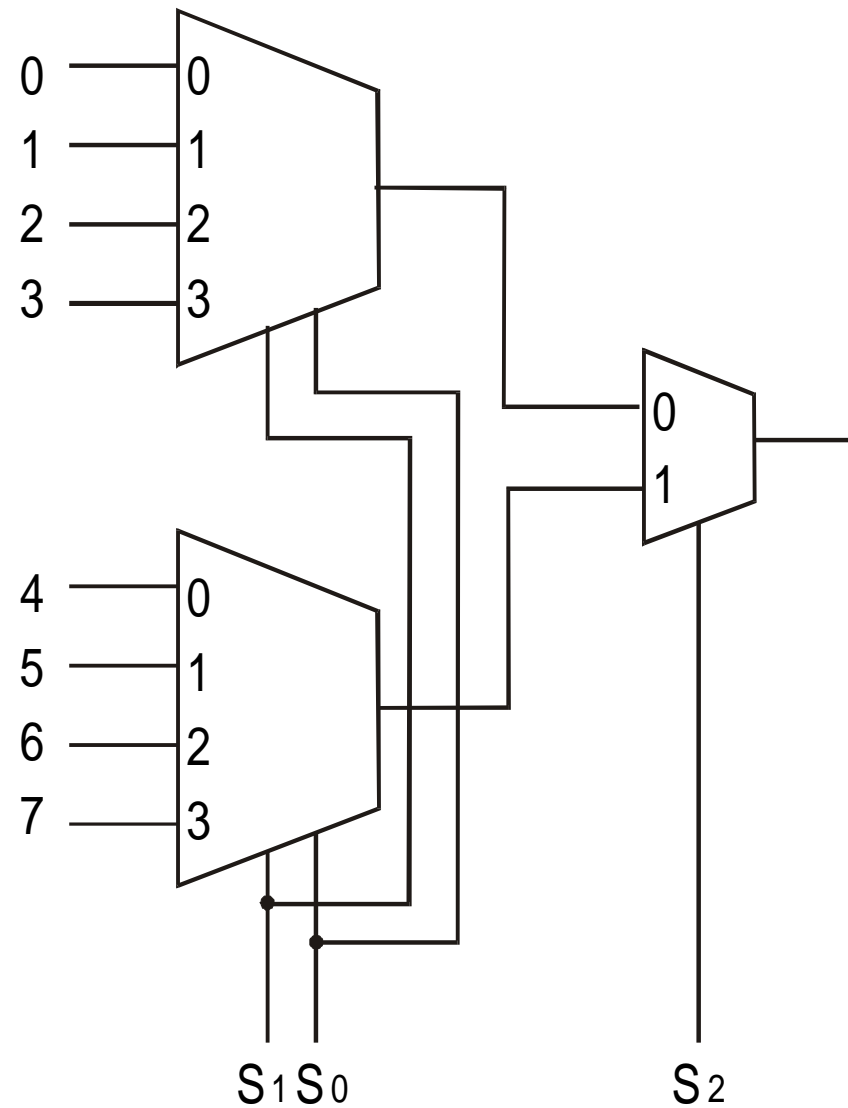


Multiplexores Comerciales



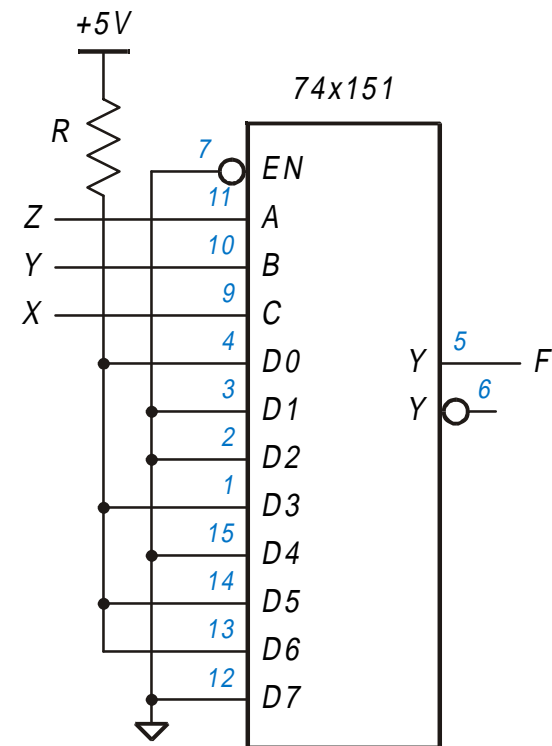
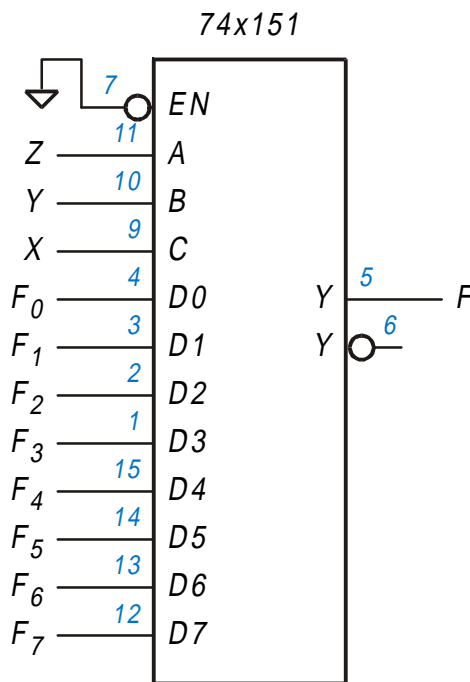
<i>Inputs</i>				<i>Outputs</i>	
<i>EN_L</i>	<i>C</i>	<i>B</i>	<i>A</i>	<i>Y</i>	<i>Y_L</i>
1	x	x	x	0	1
0	0	0	0	<i>D0</i>	<i>D0'</i>
0	0	0	1	<i>D1</i>	<i>D1'</i>
0	0	1	0	<i>D2</i>	<i>D2'</i>
0	0	1	1	<i>D3</i>	<i>D3'</i>
0	1	0	0	<i>D4</i>	<i>D4'</i>
0	1	0	1	<i>D5</i>	<i>D5'</i>
0	1	1	0	<i>D6</i>	<i>D6'</i>
0	1	1	1	<i>D7</i>	<i>D7'</i>

Expansión de Multiplexores



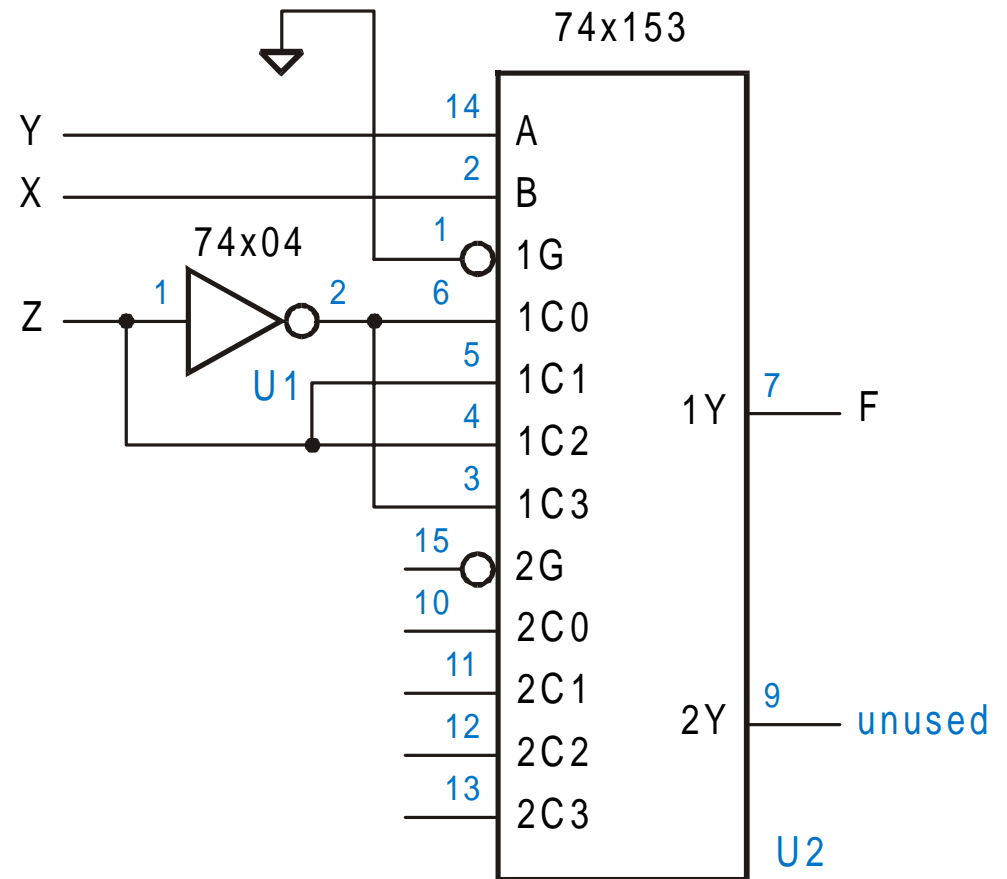
Funciones con Multiplexores

	X	Y	Z	F
F0	0	0	0	1
F1	0	0	1	0
F2	0	1	0	0
F3	0	1	1	1
F4	1	0	0	0
F5	1	0	1	1
F6	1	1	0	1
F7	1	1	1	0

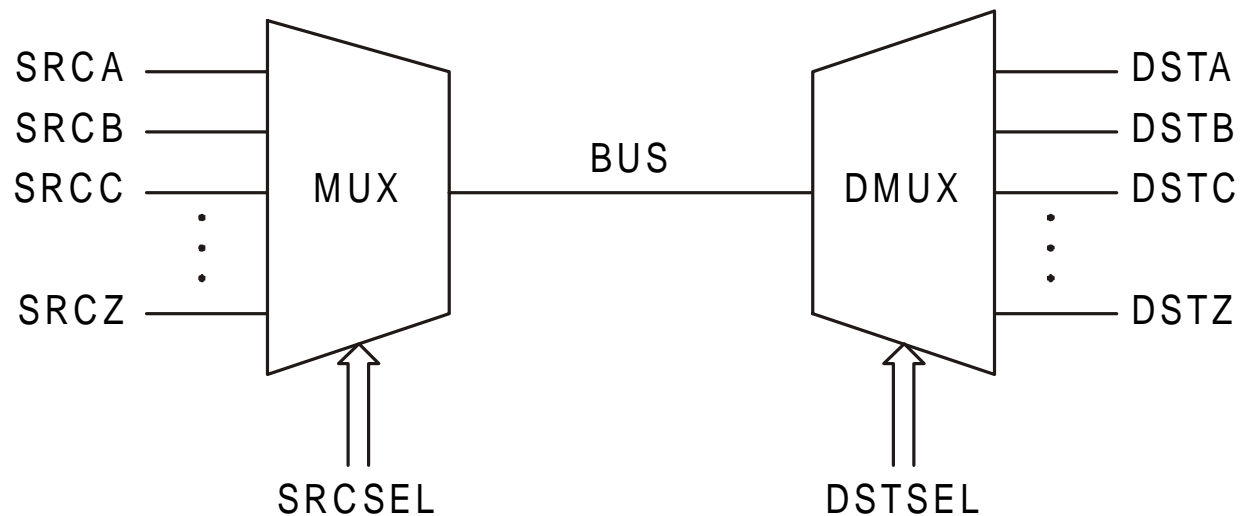
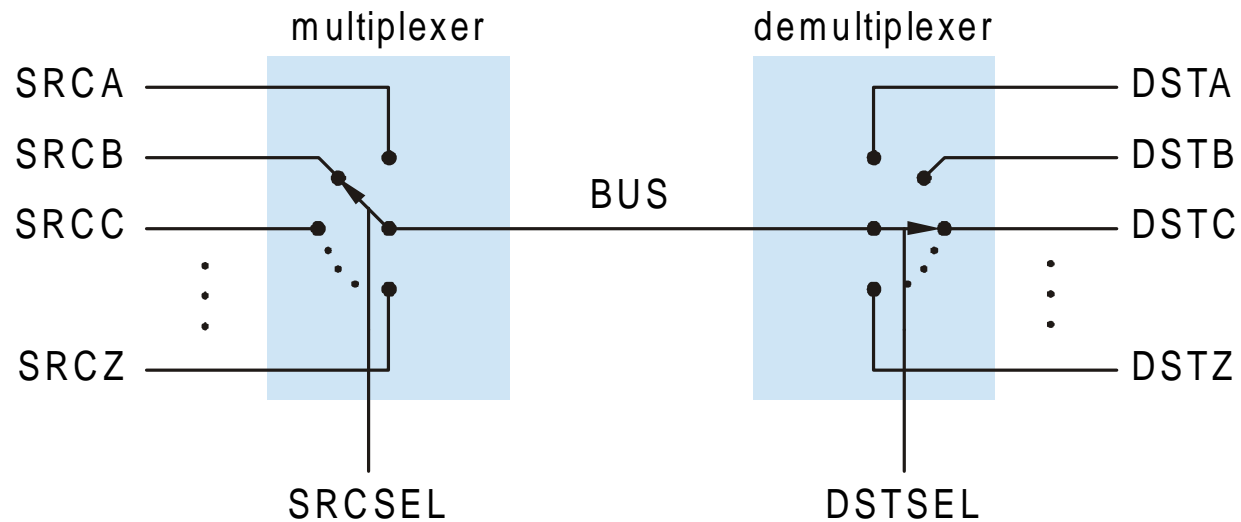


Funciones con Multiplexores

Row	X	Y	Z	F	
0	0	0	0	1	} $Z\bar{C}$
1	0	0	1	0	
2	0	1	0	0	} Z
3	0	1	1	1	
4	1	0	0	0	} Z
5	1	0	1	1	
6	1	1	0	1	} $Z\bar{C}$
7	1	1	1	0	



Demultiplexores



Demultiplexer Comercial

